Lab Project #10: Structural Design of Sequential Circuits

Revision: August 31, 2009

215 E Main Suite D | Pullman, WA 99163
(509) 334 6306 Voice and Fax

STUDENT

I am submitting my own work, and I understand penalties will be assessed if I submit work for credit that is not my own.

Print Name _____ ID Number _____

Sign Name _____ Date _____

Estimated Work Hours

1 2 3 4 5 6 7 8 9 10

Overall Weight

1 2 3 4 5 6 7 8 9 10

Point Scale

4: Exemplary
3: Complete
2: Incomplete
1: Minor effort
0: Not submitted

20% will be deducted from scores for each week late
Score = Points awarded (Pts) x Weight (Wt)

LAB ASSISTANT

#	Demonstration	Wt	Pts	Late	Score	Lab Asst Signature	Date
3	Circuit demonstration	10					
4	Circuit demonstration	10					

Total In-Lab Score

NA

GRADER

#	Attachments	Wt	Pts	Score
1	Source, simulation, worksheet	6		
2	Source and simulation	3		
3	Worksheets, source and simulation files	10		
4	Source, simulation, and worksheet	10		

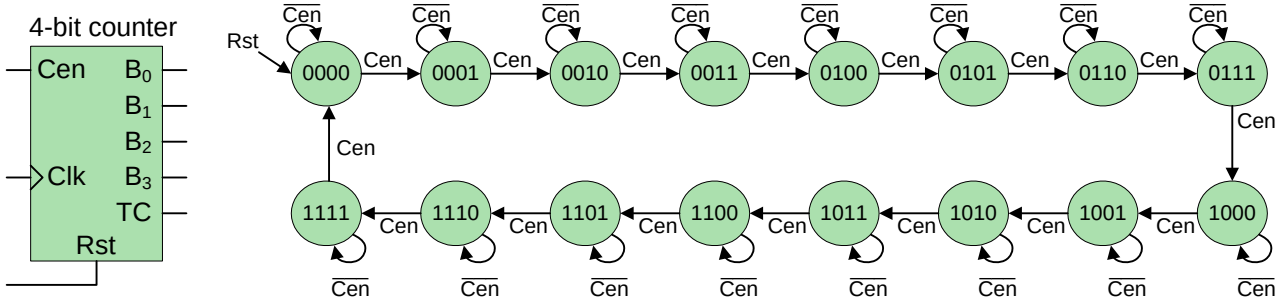
Weeks late

Total Grading Score

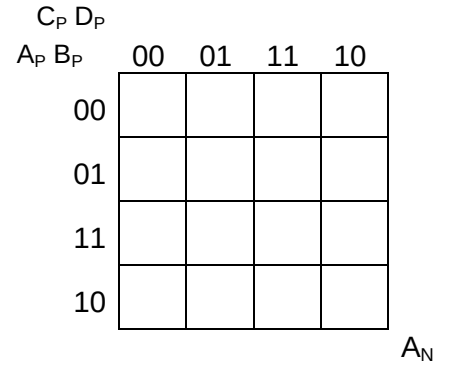
Total score is In-lab score plus grading score

Total Score

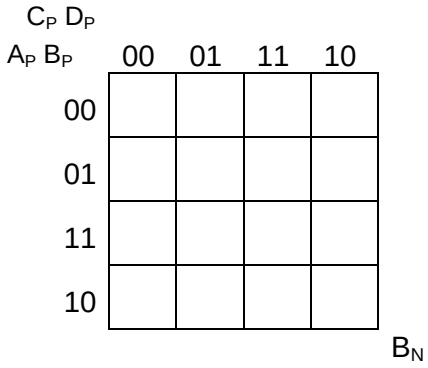
Problem 1. Using the Xilinx CAD tools, create a structural 4-bit counter with CEN and TC functions. You may use schematic methods and the FDCE flip-flop component from the Xilinx library, or structural VHDL methods (in which case you can use the flip-flop you designed in the previous lab). To complete the design, you will need to find next-state logic circuits for the counter. A state diagram and K-maps have been provided below for this purpose (or, nothing is keeping you from "borrowing" a circuit from the Xilinx schematic library, but you must complete the K-maps regardless). When the counter is complete, simulate it using a VHDL a test bench file, and be sure to show all appropriate output states. Print and submit your source and simulation files. (Hint: Extensive XOR patterns are present in the D next-state maps. You will probably want to refer to some circuit schematic source to check your K-map looping.)



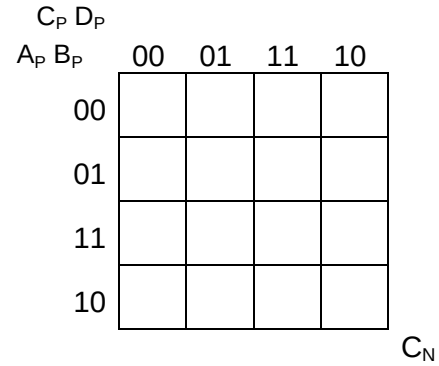
Empty K-maps follow. Note that if you choose to design a counter using DFFs with a CE input, you can ignore the CEN inputs shown in the state diagram above (i.e., the state diagram would only show branches to the next state, without any holding conditions). In this case, the counter's CEN input would directly drive the CE inputs on the DFFs (this makes the K-map loading and looping a fair amount easier – but it is your choice!).



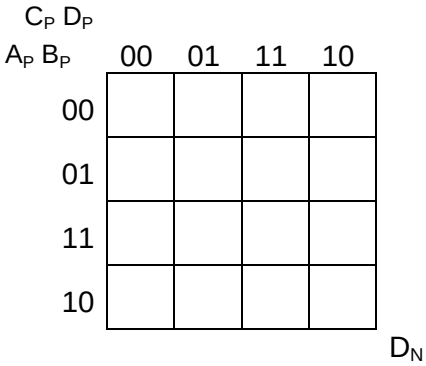
A_N = _____



B_N = _____



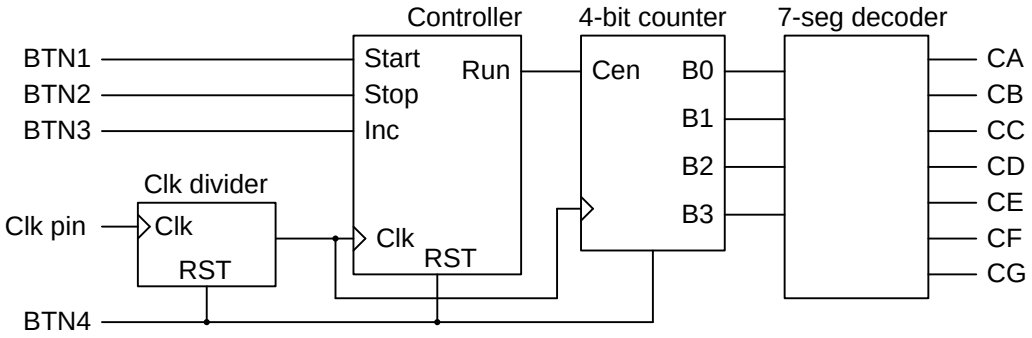
C_N = _____



D_N = _____

Problem 2. Create and simulate a behavioral VHDL 4-bit counter, using a VHDL test bench for the simulation. Print and submit your source and simulation files.

Problem 3. Design a circuit that increments a digit (0 – F) shown on the seven-segment display device once each second. The circuit has four pushbutton inputs: one button starts the counter, a second button stops the counter, a third button increments the counter, and the fourth button asynchronously resets all memory devices in the design. The system has the block diagram shown below. You must create the 4-bit counter, a clock divider, a seven-segment display decoder, and a controller circuit. You may use any design tools or methods you wish. You must also create and submit a state diagram for the controller, together with K-maps showing the next-state and output circuits. Have the lab assistant inspect your completed work, and download your design to the Digilent board. Demonstrate your circuit's function to the lab assistant and print and submit your source files for credit.



Problem 4. Modify your circuit so that all four digits on the seven-segment display are driven, and drive the least-significant digit so that it changes at a rate of once per millisecond (and so, the most-significant bit will change at a rate of once per second). This circuit requires a scanning display controller which is discussed in your board's Reference Manual. When complete, demonstrate your circuit to the lab assistant and print and submit your source files for credit. Also create and submit a detailed block diagram of your circuit showing all circuit blocks and signal connections (and make sure to appropriately label all circuit blocks and signals).